

## Notice of References Cited

Application/Control No.

Applicant(s)/Patent Under Reexamination POHLMAN, WILLIAM

Examiner

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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-5,866,924 A	02-1999	Zhu, Qing	257/208
	В	US-5,981,345 A	11-1999	Ryum et al.	438/303
	С	US-6,353,352 B1	03-2002	Sharpe-Geisler, Bradley A.	327/295
	D	US-5,861,764 A	01-1999	Singer et al.	326/93
	É	US-6,184,736 B1	02-2001	Wissell et al.	327/295
<i>,</i> •	F	US-6,211,703 B1	04-2001	Takekuma et al.	326/101
٠.	G	US-6,092,211 A	07-2000	Hozumi, Masatoshi	713/500
	Н	US-			
		US-			
	J	US-			
	κ	US-			
	L	US-			
	М	US-			

## FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	JP 10097564 A	04-1998	Japan	YAMADOU, TOSHIO	G06F 01/10
	0					
	Р					
	Q					
	R					
	s					
	Т					

## **NON-PATENT DOCUMENTS**

		NOTE ATENT DOGGILATO
*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"Clock skew reduction in ASIC logic design: a methodology for clock tree management" Balboni, A.; Costi, C.; Pellencin, M.; Quadrini, A.; Sciuto, D.; CAD of Integrated Ckts and Systems, IEEE Trans on, Vol. 17, Issue: 4, Apr. 1998, Pages:344 - 356.
	v	
	w	
	х	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.